Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A coded binary sequence, comprising:

a first group of consecutive bits, the first group having first and second separate portions and representing one of a logic 1 and a logic 0~~a first logic level~~, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of consecutive bits separate from the first group and each having a same state, the second group representing only the other of the logic 1 and the logic 0~~a second logic level~~.

2. (previously presented) The binary sequence of claim 1 wherein the first and second portions of the first group respectively comprise first and second halves of the first group.

3. (currently amended) The binary sequence of claim 1 wherein:

the first and second groups ~~logic levels~~ respectively represent ~~equal~~ logic 1 and logic 0;

the first and second states respectively equal logic 0 and logic 1; and

the second group of consecutive bits each has a state of logic 0.

4. (currently amended) A coded binary sequence, comprising:

a first group of consecutive bits each having a same state, the first group representing only one of a logic 1 and a ~~first~~ logic 0~~level~~; and

a second group of consecutive bits separate from the first group, the second group having first and second separate portions and representing the other of the logic 1 and the~~a~~ ~~second~~ logic 0~~level~~, the bits in the first portion each having a first state and the bits in the second portion each having a second state.

5. (currently amended) The binary sequence of claim 4 wherein:

the first and second groups~~logic levels~~ respectively represent~~equal~~ logic 0 and logic 1;

the bits of the first group each have a state of logic 0; and

the first and second states respectively equal logic 1 and logic 0.

6. (Original) The binary sequence of claim 4 wherein the first and second groups each respectively comprise four consecutive bits.

7. (Original) The binary sequence of claim 4 wherein the first and second portions of the second group respectively comprises first and second halves of the second group.

8. (currently amended) A coded binary sequence, comprising:

a first group of four consecutive bits each having a first state, the first group representing only one of a ~~first~~ logic 1 and a logic 0~~level~~; and

a second group of four consecutive bits separate from the first group and respectively having a second state, the second state, a third state, and the third state, the second group representing the other of the~~a second~~ logic 1 and the logic 0~~level~~.

9. (currently amended) The code word of claim 8 wherein:

the first and second groups~~logic levels~~ respectively represent~~equal~~ a logic 0 and a logic 1; and

the first, second, and third states respectively equal logic 0, logic 0, and logic 1.

10. (currently amended) A storage disk, comprising:

disk sectors operable to store application data; and

servo wedges that store servo data that includes,

a first group of consecutive bits, the first group having first and second nonoverlapping portions and representing one of a logic 1 and a ~~first~~ logic 0~~level~~,

the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of consecutive bits separate from the first group and each having a same state, the second group representing only the other of the logic 1 and thea ~~second~~ logic 0~~level~~.

11. (currently amended) A Viterbi detector operable to:

receive a signal that represents a binary sequence having a first group of consecutive bits each having a first logic level and a second group of consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing only the first logic level and the second group representing the second logic level; and

recover the binary sequence from the signal.

12. (Original) The Viterbi detector of claim 11 wherein the binary sequence comprises a coded binary sequence.

13. (Original) The Viterbi detector of claim 11 wherein:

the first logic level comprises a logic 0; and

the second logic level comprises a logic 1.

14. (currently amended) A servo circuit, comprising:

a sample circuit operable to generate samples of a signal that represents a coded binary sequence having a first group of consecutive bits each having a first logic level and a second group of consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing only the first logic level and the second group representing the second logic level; and

a Viterbi detector coupled to the sample circuit and operable to recover the coded binary sequence from the samples of the signal.

15. (Original) The servo circuit of claim 14, further comprising a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence.

16. (currently amended) A disk-drive system, comprising:

a data-storage disk having a surface, data sectors at respective locations of the surface, and servo wedges that store servo data that includes a first group of consecutive bits each having a first logic level and a second group having first and second portions of consecutive bits, the bits in the first portion having the first logic level and the bits in the third portion having a second logic level, the first group representing only the first logic level and the second group representing the second logic level;

a motor coupled to and operable to rotate the disk;

a read head operable to generate a servo signal that represents the servo data and having a position with respect to the surface of the data-storage disk;

a read-head positioning circuit operable to move the read head over the surface of the disk; and

a servo circuit coupled to the read head and operable to recover the servo data from the servo signal.

17. (Original) The disk-drive system of claim 16 wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal; and

a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal.

18. (Original) The disk-drive system of claim 16 wherein the servo circuit comprises a decoder operable to decode the recovered servo data.

19. (Original) The disk-drive system of claim 16 wherein the read head comprises a read-write head.

20. (currently amended) A method, comprising:

coding one of a logic 1 and a ~~first~~ logic 0~~level~~ as a first group of consecutive bits, the first group having first and second equally sized portions, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

coding the other and only the other of the logic 1 and the~~a second~~ logic 0~~level~~ as a second group of consecutive bits separate from the first group and each having a same state.

21. (currently amended) The method of claim 20 wherein:

the first and second groups~~logic levels~~ respectively represent~~equal~~ a logic 1 and a logic 0;

the first and second ~~logic~~ states respectively equal logic 0 and logic 1; and

the same state equals a logic 0.

22. (currently amended) The method of claim 20 wherein the coding comprises:

coding the one of the logic 1 and the logic 0~~first logic level~~ as a first group of four consecutive bits; and

coding the other of the logic 1 and the logic 0~~second logic level~~ as a second group of four consecutive bits.

23. (previously presented) The method of claim 20 wherein the first and second portions of the first group respectively comprise first and second halves of the first group.

24. (currently amended) A method, comprising:

coding a first logical bit of servo data and only the first logical bit as a first group of four consecutive bits each having a first logic level, the first logical bit representing the first or a second first logic level; and

coding a second logical bit of servo data as a second group of four consecutive bits respectively having the first logic level, the first logic level, the second logic level, and the second logic level, the second logical bit representing the first logic level if the first logical bit ~~respresents~~ represents the second logic level, the second logical bit representing the second logic level if the first logical bit represents the first logic level.

25. (previously presented) The method of claim 24 wherein:
the first logical bit equals a logic 0; and
the second logical bit equals a logic 1.

26. (Original) The method of claim 24 wherein:
the first logic level equals a logic 0; and
the second logic level equals a logic 1.

27. (currently amended) A method, comprising:

writing a first code symbol into a servo wedge of a data-storage disk, the first code symbol having a first group of code bits and a second group of code bits, having a length, and representing one of a logic 1 and a logic 0~~a first logic level~~, each bit in the first group having a first value and each bit in the second group having a second value that is different than the first value; and

writing a second code symbol into the servo wedge, the second code symbol having the length or approximately the length, having a single group of code bits each having the same value, and representing only the other of the~~a second~~ logic 1 and the logic 0~~level~~.

28. (previously presented) The method of claim 27 wherein:

the first and second code symbols each comprise a number of the code bits; and

the lengths of the first and second code symbols are each less than the product of the number and a length of a servo-bit region.

29. (Original) The method of claim 27 wherein:

the first code symbol represents a logic 0; and

the second code symbol represents a logic 1.

30. (previously presented) The method of claim 27 wherein each of the first and second groups of code words is or is approximately half as long as the first code word.

31. Cancelled.

32. (currently amended) A coded binary sequence, comprising:

a first group of consecutive bits, the first group having first and second portions and representing one of a logic 1 and a ~~first~~ logic 0~~level~~, the first portion preceding the second portion, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of consecutive bits each having a same state, the second group representing only the other of the~~a second~~ logic 1 and the logic 0 ~~level and each having a same state~~.

33. (currently amended) A coded binary sequence, comprising:

a first group of consecutive bits, the first group having first and second portions and representing one of a ~~first~~ logic 1 and a logic 0 ~~level~~, the first portion preceding the second portion, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of consecutive bits, the second group representing only the other of the~~a second~~ logic 1 and the logic 0~~level~~, all of the bits of the second group having the first state or all of the bits of the second group having the second state.

34. (currently amended) The coded binary sequence of claim 33 wherein:

the first group represents~~logic level comprises~~ a logic 1;

the first state comprises a logic 0;

the second state comprises a logic 1;

each bit of the second group has the first state; and

the second group represents~~logic level comprises~~ a logic 0.